

Appl. No. 10/709,427
Amdt. dated May 24, 2006
Reply to Office action of March 31, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 5 1 (previously presented): A chip-packaging with bonding options having a plurality of package substrates, comprising:
- a first package substrate having a high voltage or a low voltage;
 - a second package substrate having a high voltage or a low voltage, the voltage level of the first package substrate being the logical opposite of the voltage
 - 10 level of the second package substrate; and
 - a chip mounted on first package substrate, the chip comprising a plurality of bonding option pads,
 - wherein each bonding option pad of the chip is selectively connected to the first package substrate or the second package substrate.
- 15 2 (cancelled).
- 3 (previously presented): The chip-packaging of the claim 1 wherein the high voltage is the voltage of the power supply and the low voltage is the ground voltage.
- 20 4 (currently amended): The chip-packaging of the claim 1 further comprising a plurality of ~~leads~~ ~~lead-frames~~, wherein each lead ~~frame~~ is connected to one pin of the chip-packaging.
- 25 5 (original): The chip-packaging of the claim 4 wherein the pin is connected to a high voltage, a low voltage, or an input/output signal.

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6 (cancelled).

7 (original): The chip-packaging of the claim 1 wherein the first package substrate extends outside the chip and the second package substrate surrounds the chip.

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8 (previously presented): The chip-packaging of the claim 1 wherein the first package substrate and the second package substrate substantially approximate each of a plurality of the bonding pads.

10 9-18 (cancelled).

19 (previously presented): The chip-packaging of the claim 4 wherein the pin is connected to an input/output signal.

15 20 (currently amended): The chip-packaging of the claim 1 further comprising a plurality of ~~leads~~ ~~lead frames~~, each bonding option pad of the chip having a corresponding ~~lead frame~~, wherein each bonding option pad is selectively connected to the first package substrate, the second package substrate, or the corresponding ~~lead frame~~.